REMARKS

Claims 1 to 5, 7 to 9, 11 to 15, 17 to 19, 21 to 25, and 27 to 29 are pending in the application.[1] Claims 1, 9, 11, 19, 21 and 29 are independent. Favorable reconsideration and further examination are respectfully requested.

In the Office Action, all of the claims were rejected under 35 U.S.C. §102(b) over U.S. Patent No. 5,220,512 (Watkins). As shown above, Applicants have amended the claims to define the invention with greater particularity. In view of these clarifications, reconsideration and withdrawal of the art rejection is respectfully requested.

Amended independent claim 1 defines a method of modeling a logic design. The method comprises creating a graphical representation of the logic design, receiving a selection that corresponds to a type of simulation code, where the selection corresponds to one of plural different simulation languages, and generating simulation code based on the graphical representation and the selection, where the simulation code comprises executable code in one of the plural different simulation languages that corresponds to the selection. The method also includes using the simulation code to test operation of the logic design, where using the simulation code comprises propagating a state through the simulation code, and determining if there is an error in the logic design based on a propagated state. Determining is performed via executable instructions that operate absent user intervention.

The applied art is not understood to disclose or to suggest the foregoing features of claim 1, particularly with respect to receiving a selection that corresponds to a type of simulation code, where the selection corresponds to one of plural different simulation languages, and generating

[1] The Examiner is urged to independently confirm this recitation of the pending claims.

simulation code based on the graphical representation and the selection, where the simulation code comprises executable code in one of the plural different simulation languages that corresponds to the selection.

Watkins describes a system for simulating circuit designs. The Watkins system stores, in a database, software objects that define the operation of corresponding circuit elements (e.g., a flip-flop). According to the Watkins system, graphical circuit elements may be selected and interconnected to define a simulated circuit, and the simulated circuit may be stimulated with inputs to generate corresponding outputs (see Figs. 3 and 4 of Watkins). It was said in the Office Action that Watkins, column 5, lines 26 to 44, and column 5, line 59 to column 6, line 13 describe generating simulation code. Those excerpts are reproduced below:

> According to the invention, there is provided an electronic CAD system comprising a computer processor, mass storage, a display screen, means for user input, and means for circuit simulation. The electronic hardware of the means for simulation may comprise the ECAD system's computer, one or more general purpose computers interfaced to the ECAD system's computer, one or more hardware simulators interfaced to the ECAD system's computer, or any combination of these. The user interacts with the ECAD system through the use of an object-oriented user interface, whereby the user may create, select, move, modify and delete objects on the display screen, where objects may represent circuit components, wires, commands, text values, or any other visual representation of data. The graphical and software techniques of interacting with a user on such an object-oriented user interface are well known to those skilled in the art and need not be elaborated upon in this discussion.
>
> Five major software program functions run on the ECAD system: a schematic editor, a logic compiler, a logic simulator, a logic verifier, and a layout program. The schematic editor program allows the user of the system to enter and/or modify a schematic diagram using the display screen, generating a net-list (summary of connections between components) in the process. The logic compiler takes the net list as an input, and using the component database puts all of the information necessary for layout, verification and simulation into a schematic object file or files whose format(s) is(are) optimized specifically for those functions. The logic verifier checks the schematic for design errors, such as multiple outputs connected together, overloaded signal paths, etc., and generates error indications if any such design problems exist. The logic simulator takes the schematic object file(s) and simulation models, and generates a set of simulation results, acting on instructions initial conditions and input signal values provided to it either in the form of a file or user input. The layout program generates data from which a semiconductor chip (or a circuit board) may be laid out and produced.

Although it is unclear from the Office Action, Applicants assume that the Office Action is referring to the sentences underlined above in indicating that Watkins describes generation of simulation code. Even if Applicants were to concede this point (which they do not), the above excerpts of Watkins do not describe receiving a selection that corresponds to one of plural different simulation languages, and generating simulation code that comprises executable code in one of the plural different simulation languages that corresponds to the selection.

The Office Action also cites claim 1, lines 18 and 19, and claim 11, lines 36 and 37 for their disclosure of simulation code.[2] These claims, however, provide nothing that would disclose or suggest receiving a selection that corresponds to one of plural different simulation languages, and generating simulation code that comprises executable code in one of the plural different simulation languages that corresponds to the selection. Instead, the cited excerpts of the claims describe selecting a graphical object (claim 1) and representing a state of interconnections between input and output nodes (claim 11).

For at least the foregoing reasons, claim 1 is believed to be patentable over the art.

Amended independent claims 11 and 21 are article of manufacture and apparatus claims, respectively, that roughly correspond to claim 1. These claims are also believed to be allowable for at least the same reasons noted above with respect to claim 1.

Independent claim 9 includes features that are similar to those described above with respect to claim 1, and is also believed to be patentable over the art.

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[2] Since this numbering does not correspond to column line numbers, Applicants assume that the beginning of each claim is line number one, and each successive line of the claim is consecutively numbered.

Amended independent claims 19 and 29 are article of manufacture and apparatus claims, respectively, that roughly correspond to claim 9. These claims are also believed to be allowable for at least the same reasons noted above.

Each of the dependent claims is also believed to define patentable features of the invention. Each dependent claim partakes of the novelty of its corresponding independent claim and, as such, has not been discussed specifically herein.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing amendments and remarks, Applicants respectfully submit that the application is in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Applicants' undersigned attorney can be reached at the address shown below. All telephone calls should be directed to the undersigned at 617-521-7896.

No additional fees are believed to be due for this Amendment; however, if any fees are due, please charge them to deposit account 06-1050, referencing Attorney Docket No. 10559-607001.

Respectfully submitted,

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